UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,685	04/01/2004	Jeffrey Orion Pritchard	ALTRP117/A1404	1625

51501 7590 09/26/2006

BEYER WEAVER & THOMAS, LLP
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,685	PRITCHARD ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 11-16, 20-23 and 30* is/are rejected.

7)☒ Claim(s) *4-10,17-19 and 24-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/816,685 filed 04/01/2004 and amendment filed 07/21/2006.

2. Claims 1-30 remain pending in the Application.

3. Applicant's arguments have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 11-16, 20-23 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Frankel et al. (US Patent Application Publication 20030093254).

With respect to claims 1 and 30 Frankel et al. teaches a method for implementing a programmable device (within the electronic system/"system under test" being simulated (paragraph [0028]), and wherein the system under test might be a processor (programmable chip) (paragraph 0031])), a system for implementing a programmable device (within a simulation system for testing the system under test during design (paragraph [0007])), the method comprising: receiving a high-level language program, the high-level language program configured to run on a conventional central processing unit (within a node 12M as shown on the Fig. 2, wherein node represents the hardware

and software resources simulating a components of the system under test (paragraph [0030], [0056] and a programming language model 32 represents the **portion** of the system under test and is written/coded in high-level programming language such as C++, Java or **any desired programming language** (paragraph [0056] and wherein node 12M include one or more processors within computer system (paragraph [0030]), and programming language model 32 might be compiled (run) using any commercially available compiler to produce language model 32 (paragraph [0056])); identifying a portion of the high-level language program for hardware acceleration (within simulating only the portion of the system under test (paragraph [0056])); generating hardware acceleration logic for performing the portion of the high-level language program on the programmable device (within the emulator 36 shown on the Fig. 2 including hardware accelerator including plurality of PLDs such as FPGAs, which may be programmed to perform the functionality corresponding to the portion of the system under test (paragraph [0058])); and coupling the hardware acceleration logic to memory (within the simulation process running on the general computer system using their memory (paragraphs [0030], [0031])).

With respect to claim 20 Frankel et al. teaches a system for implementing a programmable device (within the system, wherein electronic system/"system under test" being simulated (paragraph [0028]), for testing the system under test during design process (paragraph [0007]), and wherein the system under test might be a processor (programmable chip) (paragraph 0031])), the system comprising: an interface operable to receive a high-level language program, the high-level language program configured

to run on a conventional central processing unit (within interface API 20 shown on the Fig. 2, node 12M, wherein API 20 is connected to the programming language model 32, which models the **portion** of the system under test, wherein the functionality of the portion is simulated and coded **in any desired programming language** (paragraph 0056] and wherein node 12M include one or more processors within computer system, and programming language model 32 might be compiled (run) using any commercially available compiler to produce language model 32 (paragraph [0030])); a processor operable to identify a portion of the high-level language program for hardware acceleration and generate hardware acceleration logic for performing the portion of the high-level language program on the programmable device (within simulating a computer system as shown on the Fig. 1, including simulating processors (paragraph [0031]) and including two or more computer system (processor units) for simulating the **portion/component** of the system under test (paragraph [0031]), wherein simulating the portion of the system under test is performed on one or more computer system (CPU) (paragraph [0006]) and the emulator 36 shown on the Fig. 2 as **hardware accelerator** including plurality of PLDs such as FPGAs, which may be programmed to perform the functionality **corresponding to the portion** of the system under test (paragraph [0058], wherein the portion of the system under test is coded in any desired programming language (paragraph [0056])).

With respect to claims 2, 3, 11-16, 21-23 Frankel et al. teaches:

Claims 2 and 22: wherein generating hardware accelerator logic includes generating HDL (within simulating a **component** of the system under test such as

portion of the system under test (paragraph [0031]) using any combination of two or more of the nodes demonstrated on the Fig. 2 (paragraph 0046]), wherein HDL description of the portion of the system under test is received (paragraph [0058]);

Claims 3, 23: wherein generating hardware acceleration logic includes generating a hardware acceleration component for implementation on the programmable device (within programmable gate arrays (FPGAs) which may be programmed to perform the functionality corresponding to the portion of the system under test (paragraph [0058]));

Claim 11: wherein the central processing unit is a general purpose processor (within simulation system which is running on the computer system (conventional CPU) (paragraphs [0006], [0030]));

Claim 12: wherein the central processing unit supports a general purpose instruction set ((within simulating a computer system as shown on the Fig. 1, including simulating processors (paragraph [0031]) and including two or more computer system (processor units) for simulating the **portion/component** of the system under test (paragraph [0031]), wherein simulating the portion of the system under test is performed on one or more computer system (CPU) (paragraphs [0006]), wherein the program is a sequence of instructions [0046[));

Claim 13: wherein the high-level language program is prepared in ANSI C (within the programming language model 32, which models the **portion** of the system under test, wherein the functionality of the portion is simulated and coded **in any desired programming language** (paragraph 0056]));

Claim 14: further comprising providing a processor core operable as a conventional central unit, the processor core configured for implementation on the programmable device (within system under test which might be processor (programmable chip) (paragraph [0031]), as demonstrated on the Fig. 10 the system under test including chip 1 and chip 2 represented by any type of models (programming language model 32) including processor core as well known on the art (paragraph [0100]));

Claim 15: wherein the portion includes multiple disconnected sections of the high-level language program (as shown on the Fig. 10 wherein the portion of the system under test is depicted having multiple portions such chip 1, chip 2 (paragraph [0100]);

Claim 16: wherein the portion is identified automatically during parsing of the hag-level language program (within the distributed simulation system having multiple nodes shown on the Figs. 1 and 2 (paragraph [0008]), wherein any combination of the nodes may be included to form the distributed simulation system (paragraph [0046]));

Claim 21: wherein the processor is further configured to couple the hardware acceleration logic to memory (within the simulation process running on the general computer system using their memory (paragraphs [0030], [0031])).

Allowable Subject Matter

6. Claims 4-10, 24-29, 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach identifying pointer access in the portion of the high-level language

program in generating hardware acceleration (claims 4-10, 24-29); a portion of the high-level language program for hardware acceleration is identified automatically using profiling data (claims 17-19).

Remarks

7. In the remarks, Applicants argue in substance:

"Frankel does not teach receiving any high-level language program or identifying any portion of a high-level language program"

8. Examiner respectfully disagrees for the following reasons:

As to argument Frankel teaches a simulation system for testing the system under test during design (paragraph [0007]), wherein simulation system is contained of multiple nodes shown on the Figs. 1 and 2 (paragraph [0008]), wherein any combination of the nodes may be included to form the distributed simulation system (paragraph [0046]) of the system under test and wherein the system under test including chip 1 and chip 2 is represented by any type of models (Fig. 10, paragraph [0100]). Moreover one of the nodes is 12M, as shown on the Fig. 2, represents the hardware and software resources simulating a **components of the system under test** (paragraph [0030], [0056] and a programming language model 32 represents the **portion** of the system under test and is written/coded in high-level programming language such as C++, Java or **any desired programming language** (paragraph [0056]. Additionally, node 12M includes one or more processors within computer system (paragraph [0030]), and programming language model 32 might be compiled (run) using any commercially available compiler to produce language model 32 (paragraph [0056]).

Based on at least these disclosures in Frankel the rejection under 35 USC § 102 is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helen Rossoshek
Examiner
Art Unit 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER